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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,573	08/09/2001	Herbert Palm	P2000,0167 US	6959

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,573	PALM ET AL.	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 27-39* is/are pending in the application.

4a) Of the above claim(s) *33-39* is/are withdrawn from consideration.

5)☒ Claim(s) *27-32* is/are allowed.

6)☒ Claim(s) *1-4,6-10,27,28 and 30* is/are rejected.

7)☒ Claim(s) *5,11-13,29,31 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *23 July 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/900,654* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/12/2004 has been entered.

Drawings

2. The proposed drawing correction filed on 07/23/03 has been approved.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4 and 6-10 are rejected under 35 U.S.C. 102(e) as being anticipated by NOGUCHI et al. (6,323,525).

Noguchi et al. discloses a memory cell comprising a semiconductor component having semiconductor material 15' and a top side, said semiconductor component being a semiconductor layer and thus selected from the group consisting of a semiconductor body and a semiconductor layer; said semiconductor material 15' having an upper surface; said semiconductor material 15' having a trench 22 (note particularly figure 25B and column 21 lines 38-48) formed therein and a gate electrode 1' (note figure 25C and column 22 line 22) located in said trench 22, a memory transistor including a source region 3 and a drain region 4 that are formed at said upper surface of said semiconductor material 15', said memory transistor including said gate electrode 1' located on said top side and located in a lateral direction between said source region 3 and said drain region 4; said source region 3 and said drain region 4 being located on opposite sides of said trench 22; a dielectric material 23 separating said gate electrode 1' from said semiconductor material 15'; and a composite film 2 of two or more of a silicon oxide film, a silicon nitride film, a tantalum oxide film, a ferroelectric film such as strontium titanate or barium titanate film forming a layer sequence including boundary layers and a memory layer located between said boundary layers, said layer sequence 2 located at least between said source region 3 and said gate electrode 1' and at least between said drain region 4 and said gate electrode 1' wherein one of said boundary layers faces said semiconductor material 15' and

at least said boundary layer that faces said semiconductor material 15' (composite film 2) may be made of tantalum oxide (Ta_2O_5), which is a material with a relative dielectric constant of at least 3.9, at least 7.8, and at least 20 (as noted in the Action mailed 04/23/2003, Chang 6,001,742 supplies the proof that Ta_2O_5 has a relative dielectric constant of at least 20, note column 3 line 24 of Chang, note further that tantalum oxide is an oxide); in the alternative that the boundary layer (being part of composite film 2) may be a silicon nitride film and thus selected from the group consisting of a nitride and an oxynitride, and wherein said memory layer (being part of composite film 2) may be tantalum oxide, strontium titanate or barium titanate, materials selected from the group consisting of undoped silicon, tantalum oxide, tantalate, hafnium silicate, hafnium oxide, titanium oxide, titanate, zirconium oxide, lanthanum oxide and aluminum oxide, and thus said memory layer may be a material selected from the group consisting of tantalum oxide and tantalate, and from the group consisting of Al_2O_3 and Ta_2O_5. Note figures 24, 25A-C, 26A, 26B, column 20 lines 24-67, column 21 lines 1-67, and column 22 lines 1-57 of Noguchi et al.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 27, 28, and 30 are rejected under 35 U.S.C.§103(a) as being obvious over BATE (4,360,900) in view of NOGUCHI et al. (6,323,525).

Bate discloses a memory cell configuration comprising a semiconductor component having semiconductor material 2 and a top side, said semiconductor component selected from the group consisting of a semiconductor body and a semiconductor layer; said semiconductor material 2 having an upper surface; said semiconductor material 2 having a plurality of trenches formed therein; a plurality of memory cells that each include a memory transistor including a source region 10a and a drain region 10b formed at said upper surface of said semiconductor material 2, said memory transistor including a gate electrode 18 located on said top side and located between said source region 10a and said drain region 10b; a dielectric material separating said gate electrode 18 from said semiconductor material 2; and a layer sequence 23-24-25 including boundary layers 23,25 and a memory layer 24 located between said boundary layers, said layer sequence located at least between said source region 10a and said gate electrode 18 and at least between said drain region 10b and said gate electrode 18; and a plurality of conductor tracks defining word lines 16, said gate electrode 18 of each one of said plurality of said memory cells electrically conductively connected to one of said plurality of said conductor tracks; said source region 10a of one of said plurality of said memory cells defining said drain region 10b of an adjacent one of said plurality of said memory cells and said drain region 10b

of said one of said plurality of said memory cells defining said source region 10a of another adjacent one of said plurality of said memory cells; said gate electrode 18 of each one of said plurality of said memory cells being located in a respective one of said plurality of said trenches, wherein: said top side of said semiconductor material 2 defines a top surface; and said layer sequence is applied completely over said top surface of said semiconductor material 2 that is between said semiconductor material 2 and said gate electrode 18 of each one of said plurality of said memory cells and that is between said semiconductor material 2 and said plurality of said conductor tracks, and wherein said semiconductor material 2 has a plurality of trenches formed therein; said gate electrode 18 of each one of said plurality of said memory cells is located in a respective one of said plurality of said trenches. Note figure 3a and column 5 lines 27-30 of Bate.

Bate does not disclose that each one of the plurality of the trenches of the memory cell configuration is shaped in a manner selected from the group consisting of being V-shaped and shaped with obliquely oriented walls formed in the semiconductor material, that the gate electrode is located in a lateral direction between the source region and the drain region, or that the source region and the drain region are located on opposite sides of each one of the plurality of trenches. However Noguchi et al. discloses a memory cell having a trench 22 shaped with obliquely (tapered at 60-89.5 degrees, note column 21 line 46) oriented walls figure formed in semiconductor material and a gate electrode 1' located in a lateral direction between a source region 3 and a drain region 4,

wherein the source region 3 and the drain region 4 are located on opposite sides of the trench 22. Note figures 24, 25A-C, 26A, 26B, column 20 lines 24-67, column 21 lines 1-67, and column 22 lines 1-57 of Noguchi et al. Note that Noguchi et al. points out (column 21 lines 32-47) that forming the gate electrode 1' in trench 22 between source 3 and drain 4 regions allows source and drain regions 3 and 4 to be formed in advance of formation of the layer sequence so that the layer sequence (Noguchi's composite film 2) is free from any influence of thermal budget necessary for activating the impurities of the source and drain regions 3 and 4, and thermal budget for the layer sequence can be small. Thus, explains Noguchi et al., a composite film of tantalum oxide or ferroelectrics (materials which "remember" their former states) such as strontium titanate, barium titanate, or lead zirconate titanate film is available for the layer sequence.

Therefore, it would have been obvious to a person having skill in the art to replace the trench, gate electrode, and source and drain of Bate's memory cell configuration with the trench, gate electrode, and source and drain such as taught by Noguchi et al. in order to reduce the thermal budget of the layer sequence to thus allow "exotic" materials such as tantalum oxide, strontium titanate, barium titanate, or lead zirconate titanate to be formed in the layer sequence.

Allowable Subject Matter

5. Claims 5,11-13,29,31, and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments with respect to claims 1-4,6-10,27,28, and 30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Mon-Thu 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for all communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD
02/2004

Minhloan Tran
Primary Examiner
Art Unit 2826